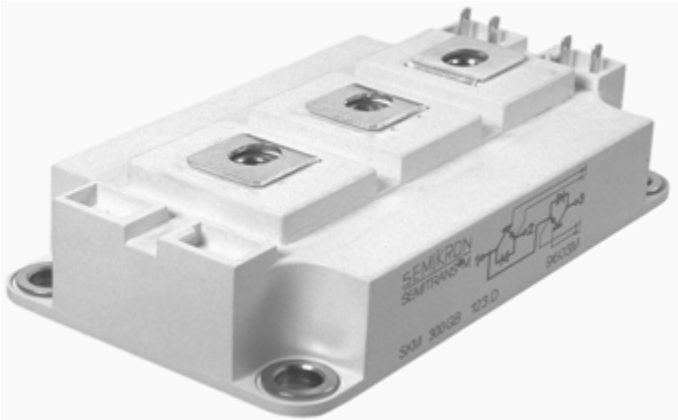
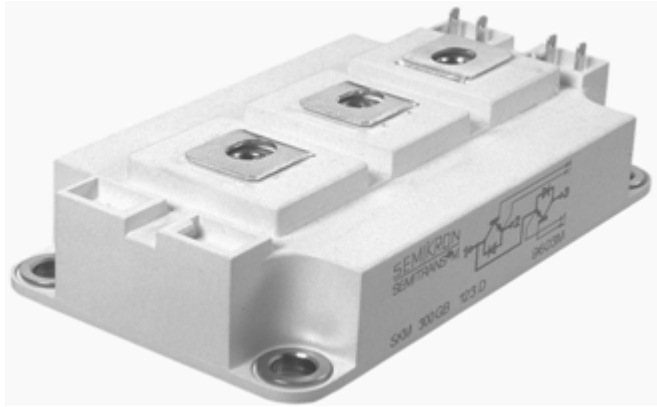
Pan Hao Co., Ltd





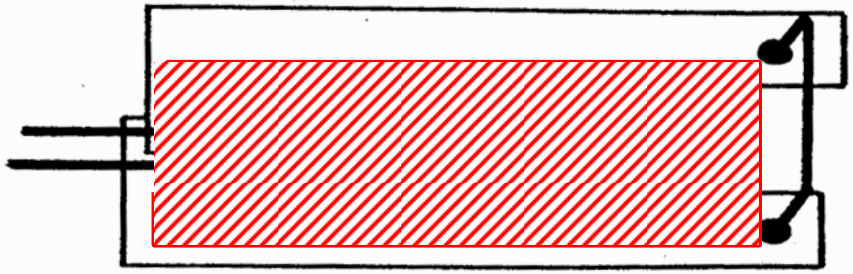
How to operate IGBT modules in parallel properly

How to operate IGBT modules in parallel properly

- Low inductive DC-link design
- Choice of right Snubber
- Low inductive and symmetrical AC-Terminal connection
- Driver properties
- Thermal management

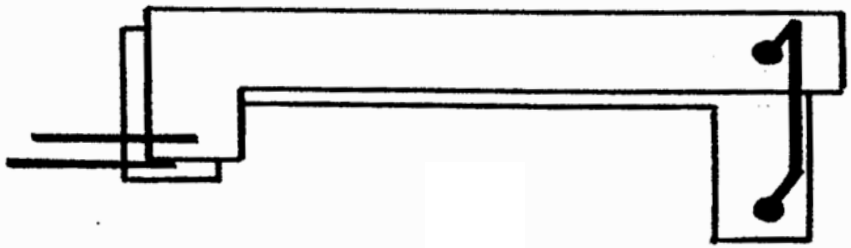
- **The mechanical design has a significant influence on the stray inductance of the DC-link**
  - The conductors must be paralleled (on top of each other), that the current has the possibility to flow as close as possible in forward and reverse direction.

L_{stray} = 100 %



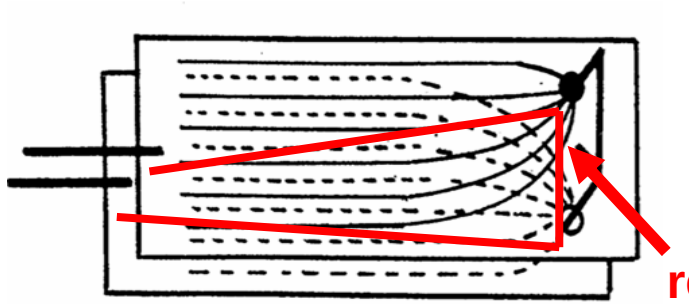
1 cm² ≈ 10 nH

L_{stray} < 20 %



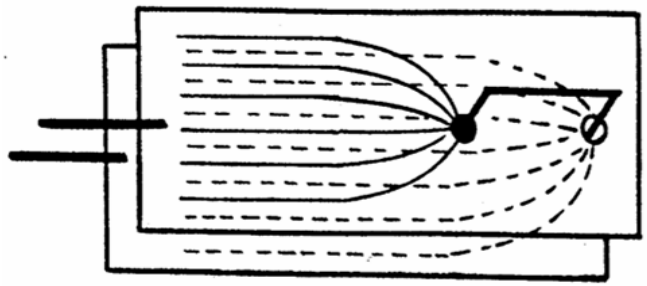
– “Sandwich” DC bus bars does not mean “low inductive” in any case
– The connections must be in line with the main current flow

L_{stray} = 100 %



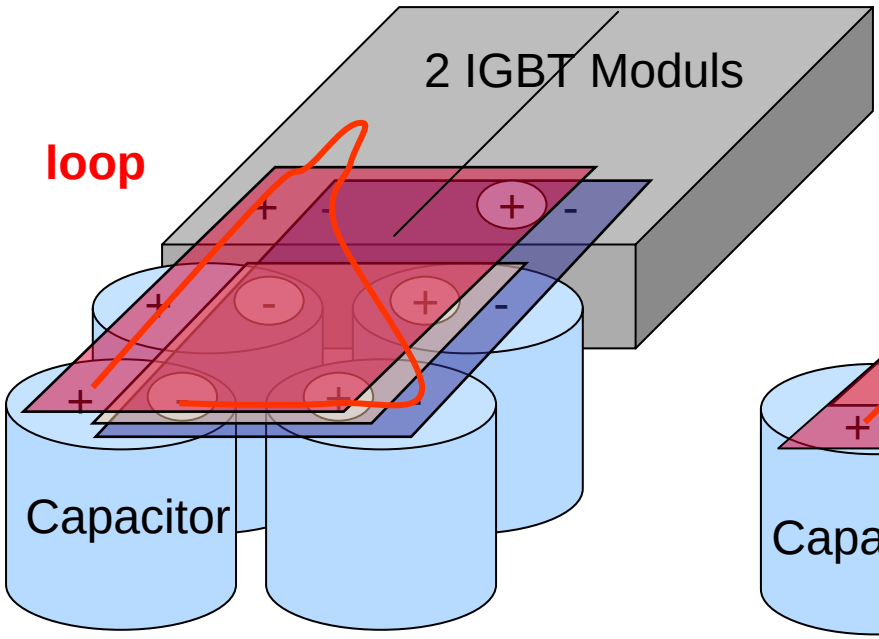
remaining loop

L_{stray} = 30 %

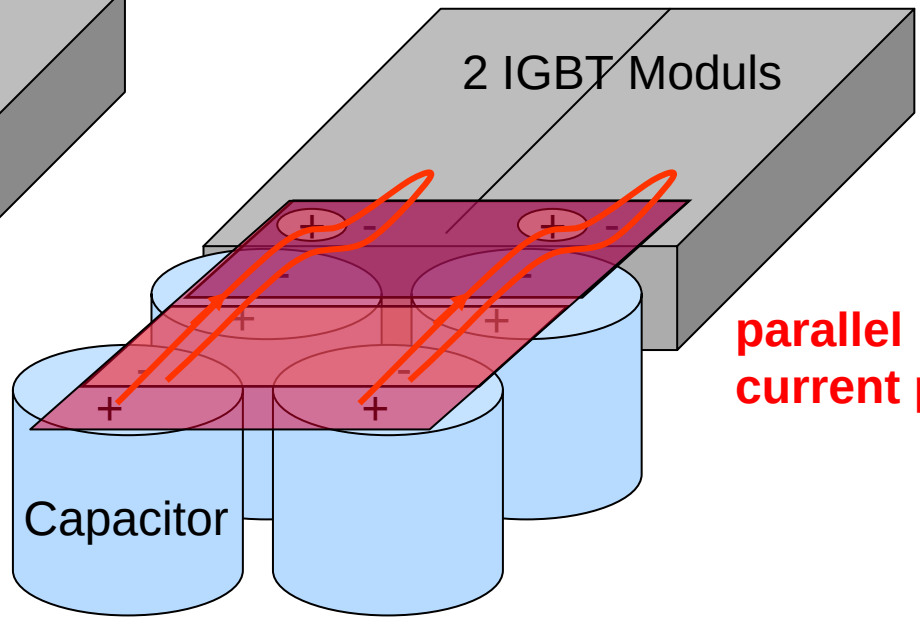


- **Comparison of different designs**
  - Two capacitors in series - two serial capacitors in parallel

Typical solution



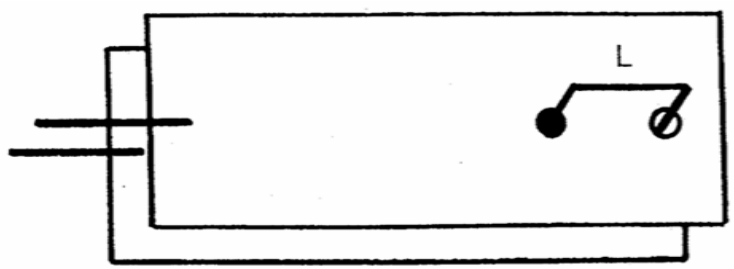
Low inductive solution



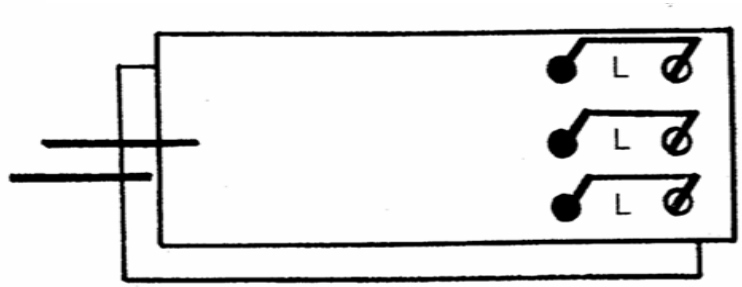
  - Each Semiconductor Module should have its “own” capacitor

- The mechanical design has a significant influence on the stray inductance of the DC-link
  - A paralleling of the capacitors reduces the inductance further

L_{stray} = 100 %



L_{stray} = 50 %



- Also the capacitors have to be decided
  - Capacitors with different internal stray inductance are available
  - Choose a capacitor with very low stray inductance!
  - Further: low “ESR” Equivalent Series Resistance
  - High “I_R” Ripple Current Capability

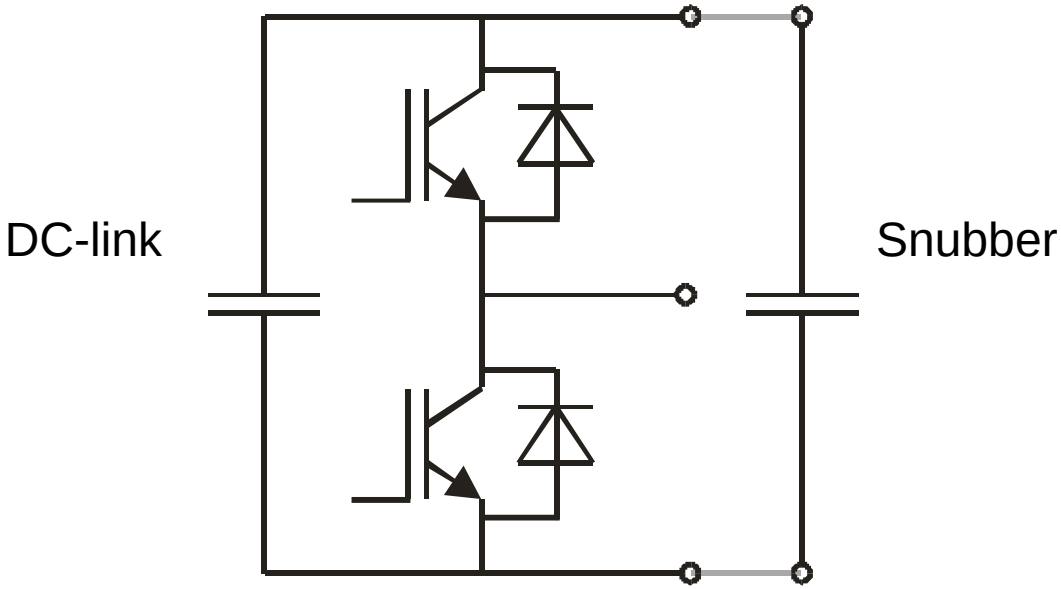
L_{stray} = ?

Ask your supplier!

How to operate IGBT modules in parallel properly

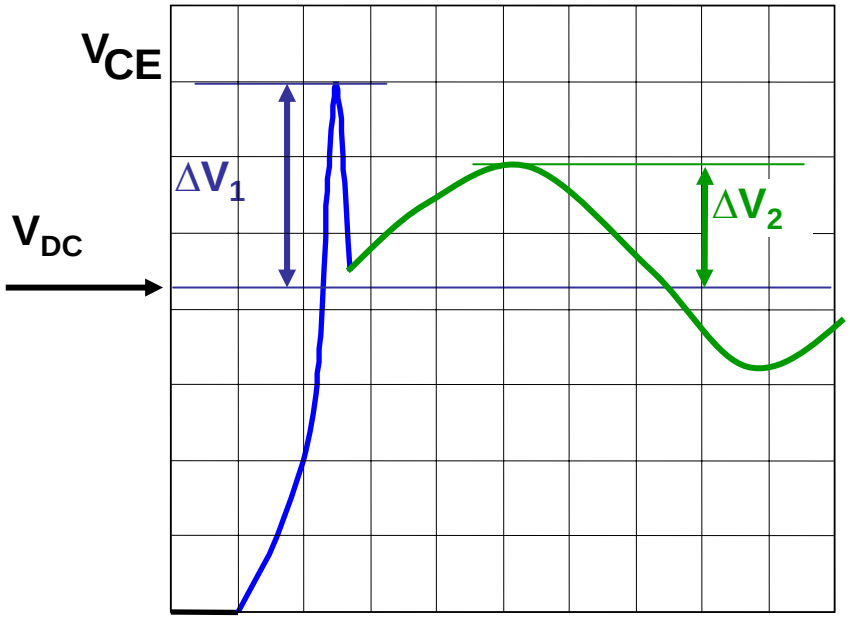
- Low inductive DC-link design
- Choice of right Snubber
- Low inductive and symmetrical AC-Terminal connection
- Driver properties
- Thermal management

- Panhao recommends for IGBT applications:
  - Fast and high voltage film capacitor ("**ISC**") as snubber parallel to the DC terminals



➔ Not to increase L_{stray}, the snubber must be located directly at DC-terminals of the IGBT module

- **Influence of DC-link stray inductance and snubber capacitor stray inductance**



$$\Delta V_1 = L_{stray-snubber} \times di_C/dt$$

$$L_{stray-snubber} = \frac{\Delta V_1}{di_C/dt}$$

$$\Delta V_2^2 = \frac{L_{stray-DC-bus} \times i_C^2}{C_{snubber}}$$

$$C_{snubber} = \frac{L_{stray-DC-bus} \times i_C^2}{\Delta V_2^2}$$

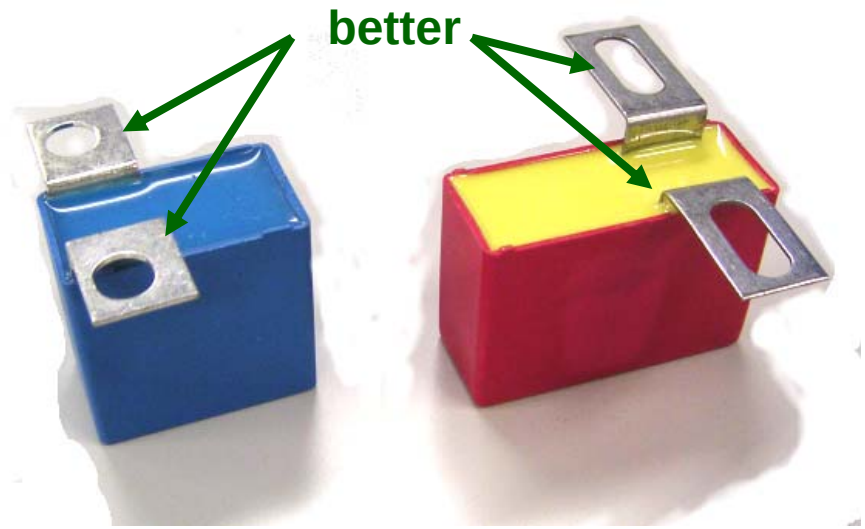
- i_C = operating current
- di_C/dt = turn off

The snubber capacitor reduces the switching voltage spike ΔV1, but can cause a ringing between DC-Link and snubber

Determination of a snubber capacitor

- From different suppliers different snubber capacitors are available.
- The different snubber capacitors have different stray inductance values. Again it is necessary to find one with lowest inductance
- In a “trial and error” process the optimum capacitance value can be found, based on measurements (0,1...0,68µF per module).

good

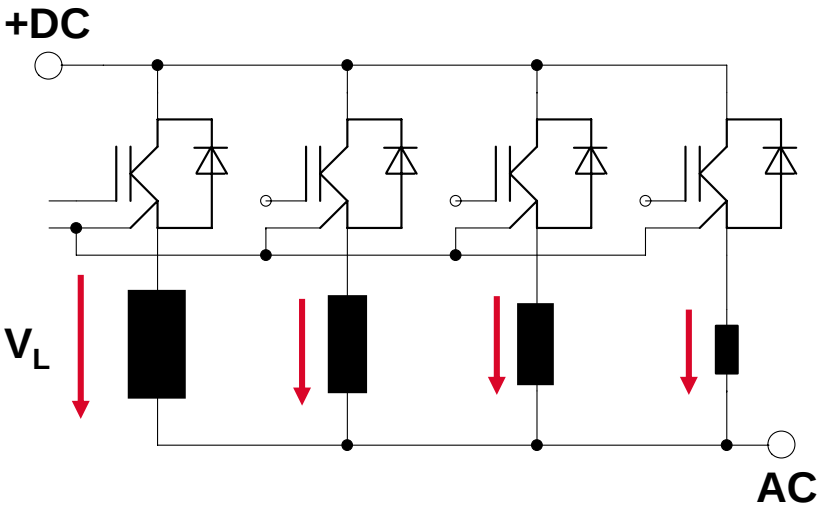


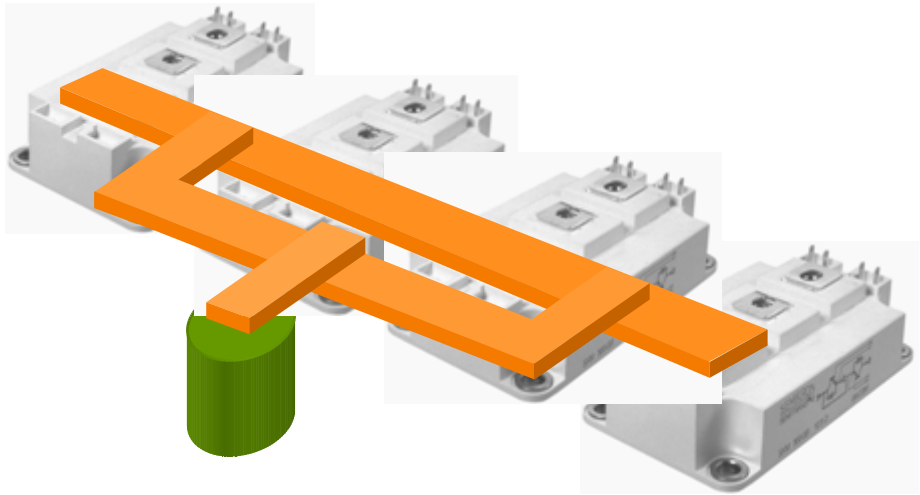
Available Snubber Capacitors

How to operate IGBT modules in parallel properly

- Low inductive DC-link design
- Choice of right Snubber
- Low inductive and symmetrical AC-Terminal connection
- Driver properties
- Thermal management

– **Short connections with identical current path length for each module**





– **Different value of LAC will induce different V_L during switching, causes:**
  - **different emitter potential of the parallel IGBT**
  - **different switching speed followed by oscillations**
  - **Loop current in Main- and Auxiliary-Emitter connections**

➔ **Look for a symmetric AC-connection so that the current sharing will be even also dynamical over all modules**

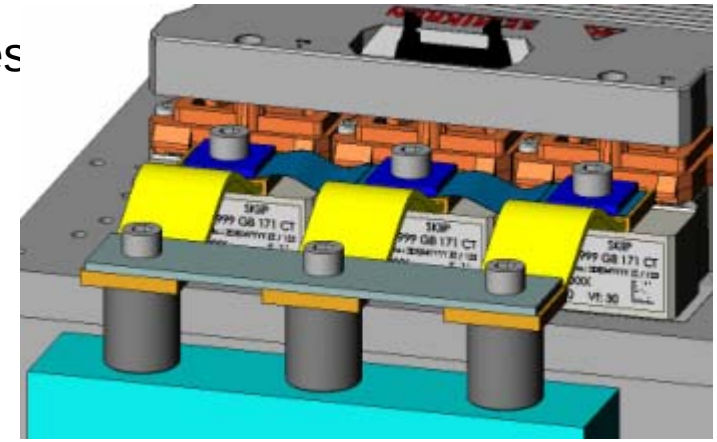
Low inductive and symmetrical AC-Terminal connection

- **AC Terminal design**

  – Flexible interconnections for large systems might be necessary to compensate differences in thermal expansion
  – Wide and thick bars for low resistances

  – ‘Long hole drillings' can compensate mechanical tolerances

  – Isolated supporting poles take over vibrations and forces from heavy AC cables

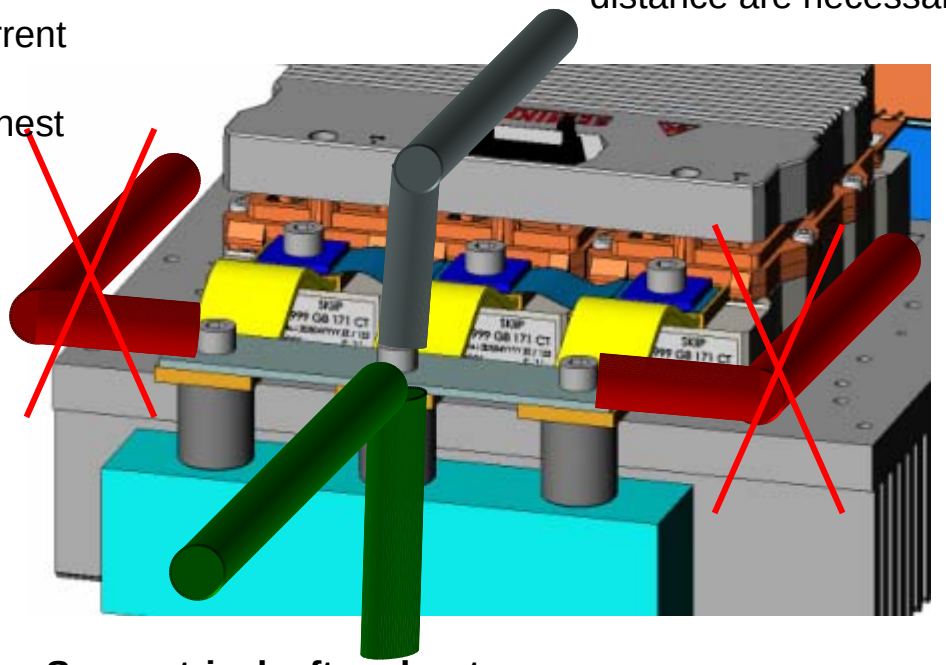


Symmetrical AC Connection

Which way should have the AC-Cable?

Symmetrical, but AC current field can disturb driver, at least 10cm distance are necessary

Unsymmetrical current loop,
Left IGBT gets highest current in case of short circuit



Unsymmetrical current loop,
Right IGBT gets highest current in case of short circuit

Symmetrical, after about 15cm the direction can change

How to operate IGBT modules in parallel properly

- Low inductive DC-link design
- Choice of right Snubber
- Low inductive and symmetrical AC-Terminal connection
- Driver properties
- Thermal management

Important driver properties for parallel operation

- The maximum driver gate charge $Q_{G(max)}$ must be greater than $n*Q_G$ or the total gate resistor R_G/n must be greater than the minimum driver gate resistor value $R_{G(min)}$, otherwise the gate voltage breaks down

- The average current I_{av} of the driver power supply has to be greater than $n*Q_G*f_{sw}$ (n – number of parallel devices; Q_G – gate charge; f_{sw} - switching frequency

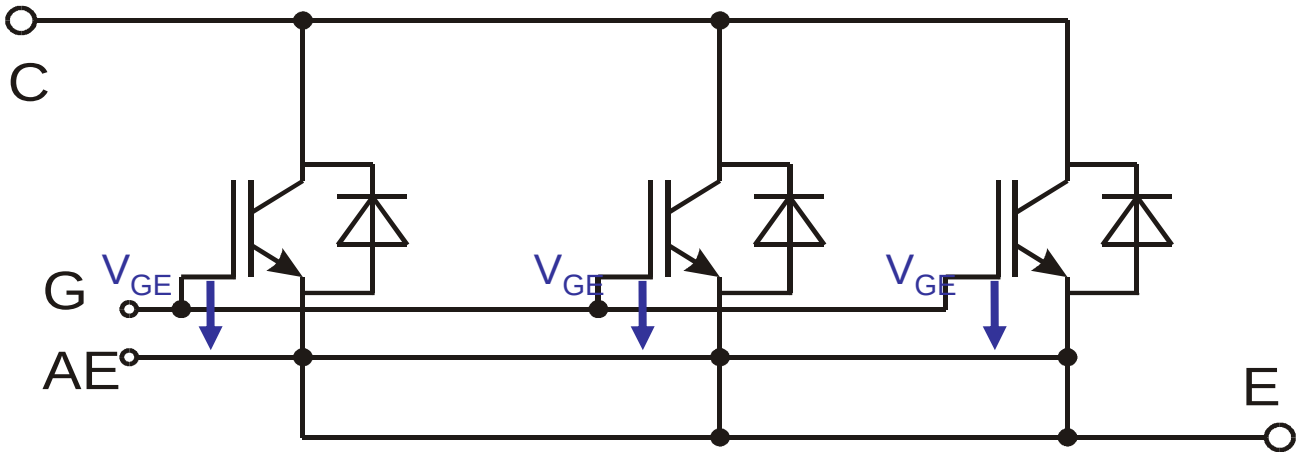
- Same propagation delay time (dead time) for all parallel channels as well as for TOP and BOTTOM IGBT

Other driver features

- Insulation primary/secondary side
- Interlock between TOP and BOTTOM IGBT
- Short pulse suppression
- Protection function (to high temperature, over current, power supply monitoring)
- Extreme high noise immunity (EMC)

- **Different IGBT modules with different electr. characteristics**

  (t_{on} and t_{off}; $V_{GE(th)}$; Q_G ; „Miller Capacity“ C_{res} and Transfer characteristic $I_C = f(V_{GE})$

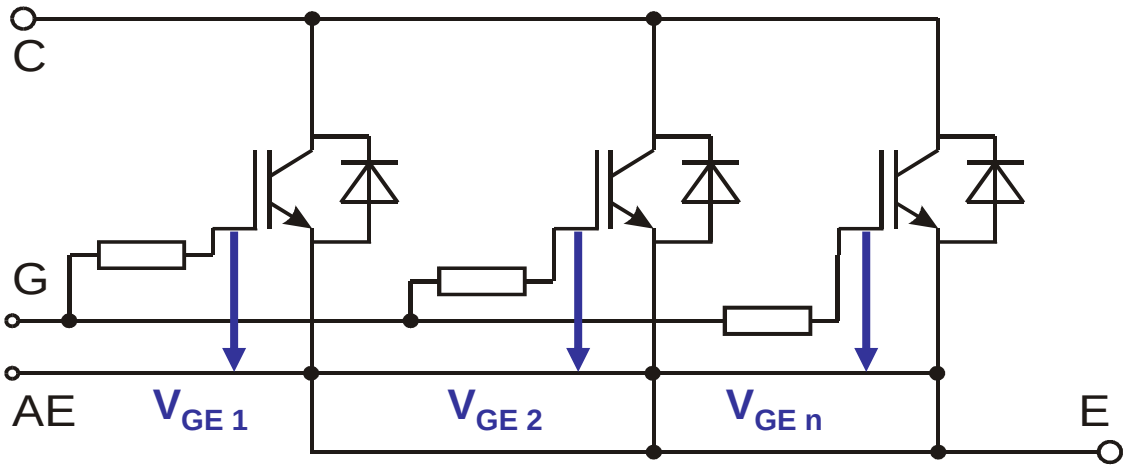


Due to hard connected gates, all IGBT must have the same V_{GE}
This means: IGBT do not switch independently from each other

- The IGBT with the lowest $V_{GE(th)}$ turns on first.
- The gate voltage is clamped to the Miller-Plateau. Therefore IGBT with higher $V_{GE(th)}$ can not turn on.
- The IGBT with low $V_{GE(th)}$ takes all the current and switching losses during turn on.

Worst Case: All Contacts Shorted

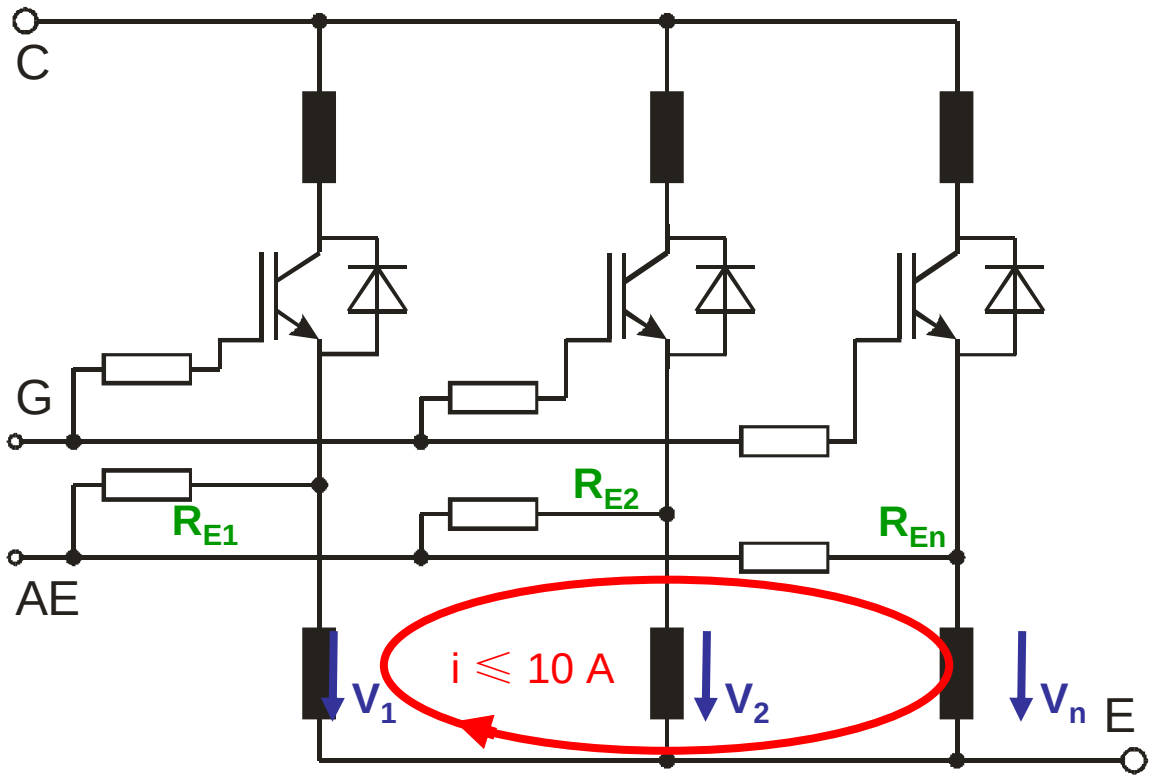
- **Separated by gate resistors**
  - The gate voltage of each IGBT can rise independent from the other one. The individual threshold voltage can be reached nearly simultaneously.



- Sophisticated gate resistor optimisation, → to fast: high differences in the current sharing during switching, → to slow: high losses and high risk of oscillations during active IGBT mode (in the range of $V_{GE(th)}$ at switching or in short circuit mode)
- may be individual optimisation of $R_{G(on)}$ and $R_{G(off)}$
- Note: The gate resistors must be tolerated < 1 %

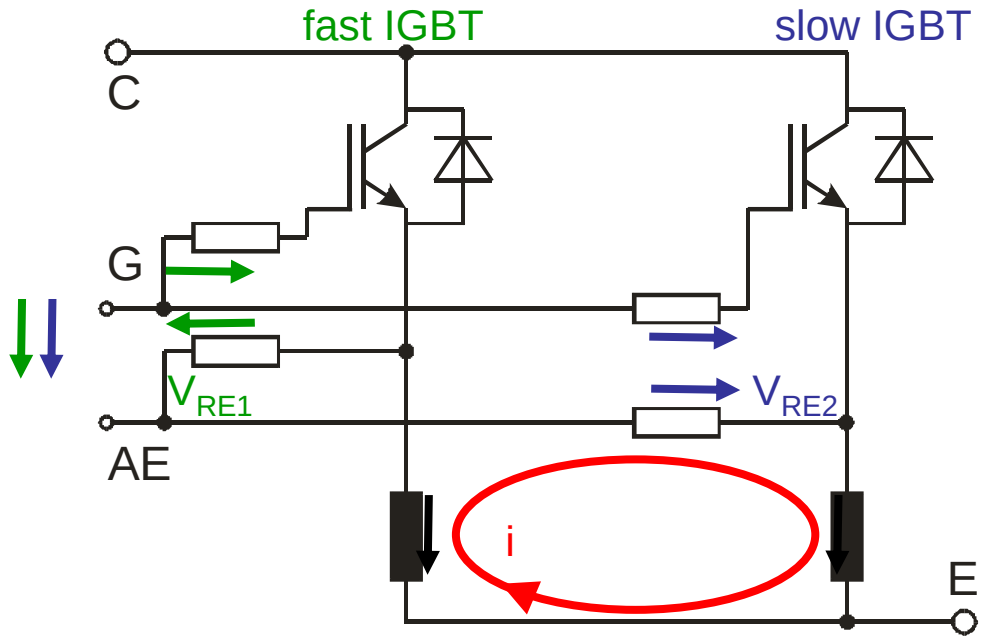
Separate Gate Resistors for parallel Connection

- **The introduction of R_{Ex} ($\approx$ 10 % of R_{Gx} but min. 0,5 Ω) leads to**
  - Limitation of equalising currents i $\leqslant$ 10 A
  - Damping of oscillations

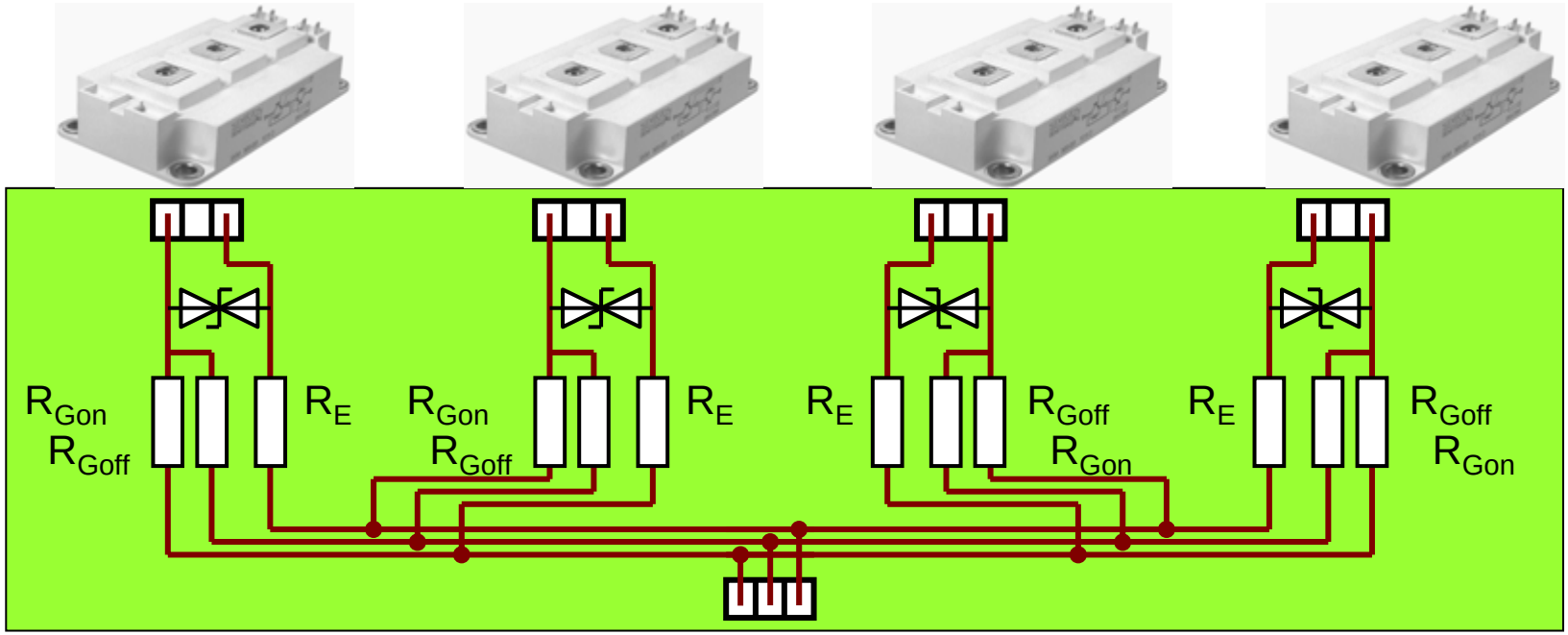


Introduction of Auxiliary Emitter Resistors

- **The introduction of R_{Ex} leads also to a negative feedback**:
  - The voltage drop V_{RE1} reduces the gate voltage of the fast IGBT and decreases therewith its switching speed.
  - The voltage drop V_{RE2} increases the gate voltage of the slow IGBT and makes it faster.
  - During switch off: vice versa.



- PCB for paralleling IGBT close to the module connectors
- Same track length on the board (= same inductances) for all IGBT
- Option of individual $R_{G(on)}$, $R_{G(off)}$ and gate clamping
- Short, twisted pair wires from the board to the modules ($\leqslant$ 5..10 cm)



Parallel Board for parallel modules to distribute Gate signals

How to operate IGBT modules in parallel properly

- Low inductive DC-link design
- Choice of right Snubber
- Low inductive and symmetrical AC-Terminal connection
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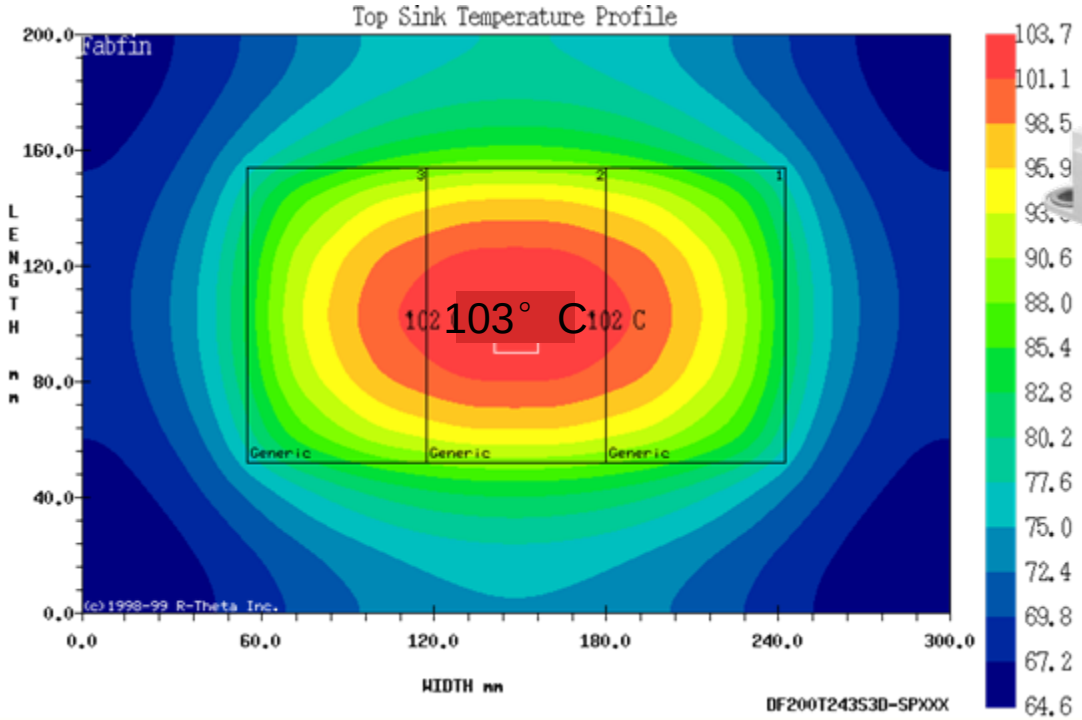
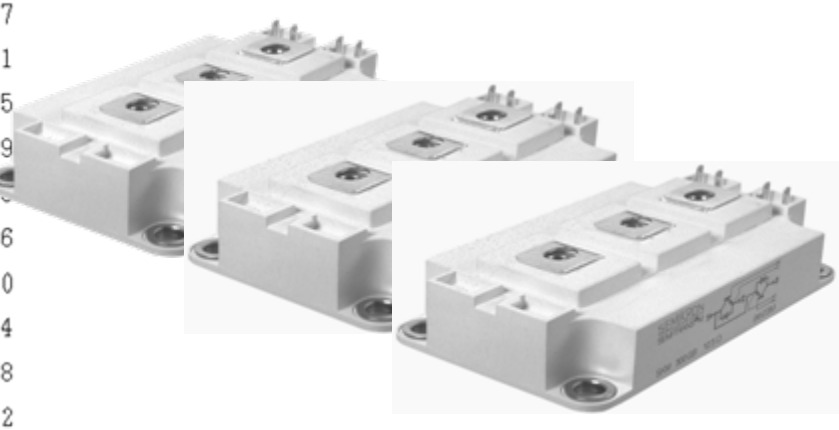
- Thermal management

- **Taking thermal management into regard**
  - No space between the paralleled modules lead to low stray inductances and minimum space
  - But the thermal stacking makes a current de-rating necessary

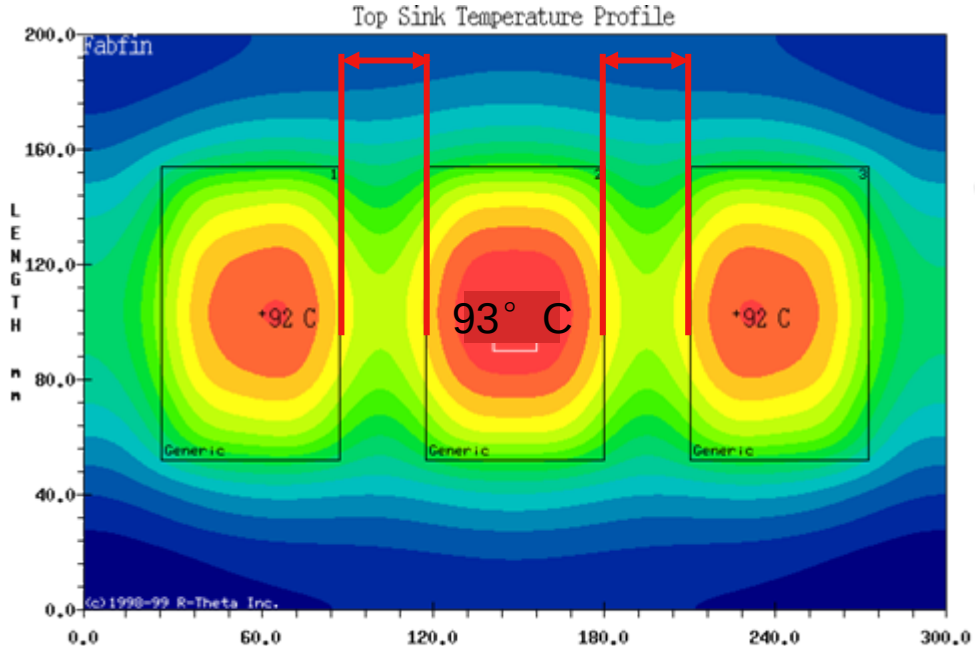


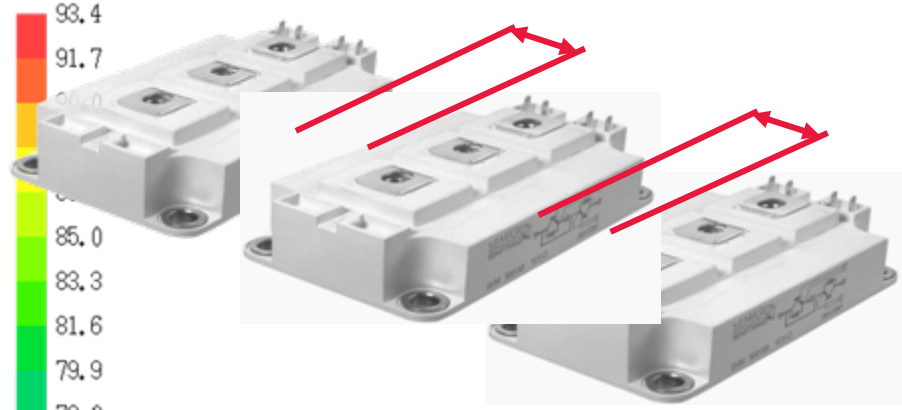


$$R_{th(s-a)} = \frac{103°C - 40°C}{1500W} = 0.042K/W$$

Reduction of T_j by higher heat sink efficiency

- 20 – 30 mm space between the modules
  - increase the inductances but
  - Increase the heat sink efficiency significantly (reduces the thermal resistance, shown Example: reduction by 17%)





$$R_{th(s-a)} = \frac{93°C - 40°C}{1500W} = 0.035K/W$$

➔ Optimised thermal management leads to maximum possible current ratings

Reduction of T_j by higher heat sink efficiency